Reduced Components Dual-Module Multilevel Inverter with Symmetric and Asymmetric Configurations

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Abstract—In this study, a dual-module MLI is presented which is based on the single construction from a previous topology. The presented MLI offers reduced number of controlled power switches compared with recent topologies. Also, the proposed inverter offers low total standing voltage as it provides the overall cost of the presented topology. Reductions of power switches count, reduced blocked voltage across power switches in addition to decreased number of DC voltage sources are considered the main advantages of the proposed dual-module MLI topology. Level shifted pulse-width modulation technique is adopted for generating the switching signals of the power switches. To validate the merits of the proposed topology, a comparison study with recently published topologies is performed under symmetric configuration in terms of the value of blocked voltage and total count of components e.g. switches, dc voltage sources, diodes. The operation of the dual-module topology is examined by the nine and thirteenth -level configurations employing only ten power switches. Simulation results are carried out to present the validation of the proposed topology. In addition, real time system using dSAPCE 1103 as a controller has been used to ensure the validity of the inverter. The proposed inverter offers low harmonic contents in the inverter output voltage with lower components count.

Index Terms—Multi-Level Inverter; Level shifted; Single-Phase Inverter; Total Standing Voltage; Total Harmonic Distortion

1 Introduction

Voltage source inverter (VSI) are undoubtedly the key element in utilization of many medium/high power industrial applications, such as photovoltaic generation systems (PVGS) [1], Ac drives [2], uninterruptable power supplies (UPS) [3], …etc. Since the invitation of multilevel inverters (MLIs) which was first introduced in 1975 [4], the global demand has been grown in the last two decades in the field of DC/AC power conversion technology [5]. It provides AC voltage characterized by low total harmonic distortion, high modularity and smaller filter size in comparison with traditional three-level VSI [6], [7].

MLI has the ability to synthesize nearly sinusoidal waveform with improved harmonic spectrum. If the amount of levels is extended to infinity, the total harmonic distortion (THD) for the output voltage of MLI leads to zero [8]. MLI is the structure of multiple input DC levels which is obtained from separate DC voltage sources and/or DC bus capacitors, and power semiconducting devices.

The emergences of MLI started with traditional MLI topologies, namely, flying capacitors (FC) [9], [10], neutral point clamped (NPC) [11], and cascaded H-bridge (CHB) [12]. MLI are restricted by application, cost, used components and complexity. The selection of used topology and the number of levels depends mainly on the system power and voltage ratings, cost, and mainly on inverter's efficiency. In order to obtain higher levels, NPC and FC topologies suffer from requiring increased number of diodes and clamping capacitors, respectively.

Among these topologies, CHB becomes the most attractive topologies as it provides modularity for higher voltage levels with low number of components and high efficiency. However, CHB possess some drawbacks as for increasing the number of output voltage levels, the number of switching components, along with peripheral devices such as gate drive circuits and heat sinks, increases. In addition, the cost, losses, and complexity of the overall system will increase. CHB are further classified into symmetrical and asymmetrical topologies based on values of DC voltage sources. Asymmetrical configurations using unequal DC voltage sources provide higher number of voltage levels as compared with symmetric configurations having the same number of components [13]. However, they still require high number of components.

Consequently, in the past few years, researchers paid great effort to evolve new topologies with less components and complexity to overcome problems associated with CHB in symmetric and asymmetric topologies. Some of these topologies are reviewed here briefly. Topology of MLI based on multi-winding transformer was proposed on [14] that can be used for medium voltage application. It uses three phase inverter modules along with an output transformer which can be employed for high power applications but at increased cost and complexity. Four DC sources were used to obtain five-level in [15] , whereas the same number of sources can be used to generate higher levels in conventional topologies. In [16], a coupled inductor is used with six power switches to generate five-level output voltage. However, the overall cost, size, and weight have been increased. In [17], another topology was presented for four-level inverter, however, this topology is valid only for even voltage levels and is unable to provide zero-level which exhibits high significant harmonic energy concentrated at switching frequency. Another topology for generating five-level was presented in [18], however, the system doesn't provide modularity for higher voltage levels.

Most of topologies have been presented in literature survey reflects the fact of using lower number of components for obtaining higher levels. Conversely, a great concentration has been made in terms of simplicity, losses, and modularity. Therefore, this paper focuses on proposing a MLI topology

based on modular structure and offers lesser number of components and reduced blocked voltage across power switches. The proposed inverter is studied using the dual-module MLI which is connected using two single-module circuits modified from topology presented in [19], [20] and a modified H-bridge circuit. The proposed inverter is tested to generate nine and thirteen output voltage levels as a symmetry and asymmetry topologies, respectively. A comprehensive comparison has been carried out between the proposed dual-module inverter and recent topologies with reduced components count in the symmetrical configuration to highlight merits of the proposed inverter.

The paper organization is as follows; proposed MLI topologies with dual-module is presented in section 2 using two cells to provide different voltage levels configuration, its operating modes, and switching states. Section 3 deals with the modulation scheme used to generate the switching signals. Section 4 presents the simulation results and validated with real-time results which is presented in Section 5. The comparison of symmetrical topology to the earlier presented topologies is provided in Section 6. Finally, the conclusion is given in Section 7.

2 Configuration of the Proposed Dual-Module Multilevel Inverter

2.1 General structure

Fig. 1 presents the structure of the proposed Dual-module MLI. It consists of two main parts. The first part is the hexagon switch cell (HSC) which is a traditional H-bridge but the two legs are separated by two power switches. The second part is the two single-modules (I, II), which are based on single-module auxiliary circuit MLI proposed in [19], [20]. It can be seen that the single-module structure is reduced by one power switch compared with the aforementioned topology. Both modules are responsible of generating different voltage levels at the end of HCS where each module consists of an 'n' number of cells. Each cell includes one DC source and one unidirectional switch. Switches of the 2nd cell to the nth cell have no fast recovery diode to avoid short circuit between DC sources.

In module-I, the 1st cell has one DC source and one unidirectional switch with a fast recovery diode. The function of diode in the 1st cell is to produce the first levels, i.e. $\pm V_{dc}$, while the function of the power switch is to provide a freewheeling path to avoid serve voltage build up across the power switch in case of inductive loads as will be seen in the next section. In contrast, the first cell in module-I doesn't exist in module II as shown in Fig. 1.

If the two modules have the same number of cells, there are 'n' DC sources in either of the modules. The values of DC voltage source in module-I and module-II are presented in the following equations.

In module-I: $V_{1L}=V_{2L}=V_{3L}=\cdots=V_{nL}=V_{DC}$ (1)

In module-II: $V_{1R}=V_{2R}=V_{3R}=\cdots=V_{nR}=\beta V_{DC}$ (2)

where, $\beta = 1, 2, 3\ldots n+1$, also number of levels (N_{Levels}) and number of power switches (N_{Sw}) for dual-module MLI will be:

$N_{Levels}=2n(\beta+1)+1$ (3)

$N_{Sw}=2n+6$ (4)

One of the most considering parameter in designing of inverter is the blocked voltage across each power switch used. The blocked voltage determines the power rating of switch, as the power rating of power switches increased, the cost will in turn increases. In the proposed dual-module MLI, the blocking voltage in power switches are as provided in the following equations:

$Vb_{S1L}=Vb_{S2L}=Vb_{S3L}=\cdots=Vb_{SnL}=V_{DC}$ (5)

$Vb_{S1R}=Vb_{S2R}=Vb_{S3R}=\cdots=Vb_{SnR}=\beta V_{DC}$ (6)

$Vb_{Q1}=Vb_{Q4}=n*V\_{DC}$ (7)

$Vb_{Q2}=Vb_{Q3}=n*\beta V_{DC}$ (8)

$Vb_{Q5}=Vb_{Q6}=V_{abmax}=n*(1+\beta)V_{DC}$ (9)

It is important to mention here that only two power switches i.e. Q_5, Q_6 have to withstand the full rated output voltage As shown in (9) which in turn limits its application for high voltage applications. Therefore, the total cost is reduced to a considerable amount. The merit of any topology is defined by calculating total standing voltage (TSV). TSV is the sum of blocking voltage across each power switch. In dual-module, TSV will be:

$TSV= 5n*(1+\beta)V_{DC}$ (10)

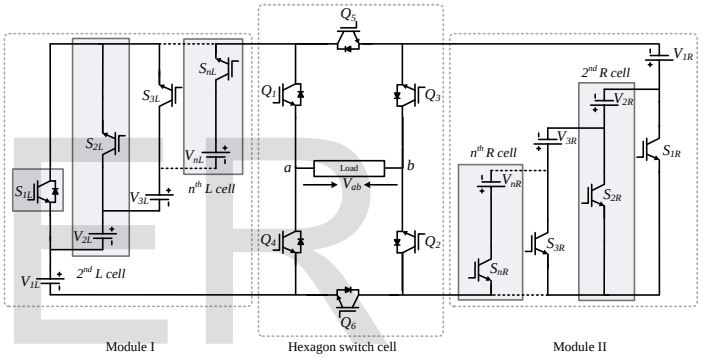


Fig. 1. Proposed Dual-Module MLI

2.2 Two-Cell Dual-Module Multilevel Inverter

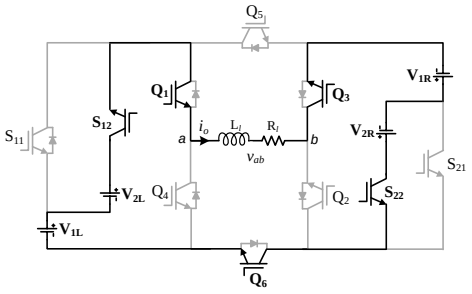
In this section, dual-module MLI is examined with two cells (n=2) in each module.

2.2.1 Symmetrical Dual-Module MLI

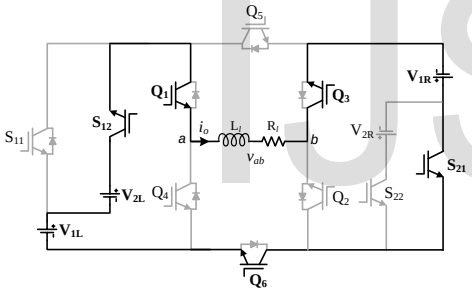
For symmetrical configuration, β equals to '1' where DC voltage sources have equal magnitudes. According to number of cells and value of DC voltage sources, the proposed topology provides nine-level at the inverter terminals as presented from (3). The configuration of the nine-level inverter is illustrated in Fig. 1. As shown, it consists of four DC sources with equal magnitudes ($V_{1L}=V_{2L}=V_{1R}=V_{2R}=V_{DC}$) and ten power switches based on (4). Table 1 presents the switching states to obtain symmetrical nine-level. The operating modes for the generated output levels are described in Fig. 2.

TABLE 1
SWITCHING STATES OF SYMMETRICAL NINE-LEVEL INVERTER

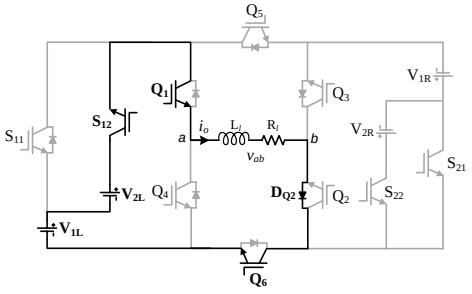
Voltage levels	Voltage magnitude	Switching states
$4V_{dc}$	$V_{1L}+V_{2L}+V_{1R}+V_{2R}$	$S_{12}, Q_1, Q_3, S_{22}, Q_6$
$3V_{dc}$	$V_{1L}+V_{2L}+V_{1R}$	$S_{12}, Q_1, Q_3, S_{21}, Q_6$
$2V_{dc}$	$V_{1L}+V_{2L}$	S_{12}, Q_1, D_{Q2}, Q_6
$V_{dc}(+)$	V_{1L}	$D_{S12}, Q_1, D_{Q2}, Q_6$
$V_{dc}(-)$	V_{1L}	$S_{11}, D_{Q1}, Q_2, D_{Q6}$
0(+)	-	D_{Q2}, D_{Q4}, Q_6
0(-)	-	Q_2, Q_4, D_{Q6}
$-V_{dc}(-)$	V_{1L}	$D_{S11}, Q_4, D_{Q3}, Q_5$
$-V_{dc}(+)$	V_{1L}	$S_{11}, D_{Q4}, Q_3, D_{Q5}$
$-2V_{dc}$	$V_{1L}+V_{2L}$	S_{12}, Q_4, D_{Q3}, Q_5
$-3V_{dc}$	$V_{1L}+V_{2L}+V_{1R}$	$S_{12}, Q_4, Q_2, S_{21}, Q_5$
$-4V_{dc}$	$V_{1L}+V_{2L}+V_{1R}+V_{2R}$	$S_{12}, Q_4, Q_2, S_{22}, Q_5$



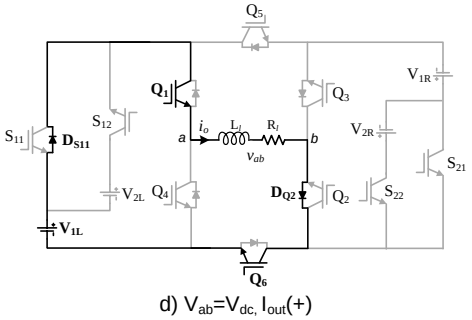
a) $V_{ab}=4V_{dc}$, $I_{out}(+)$



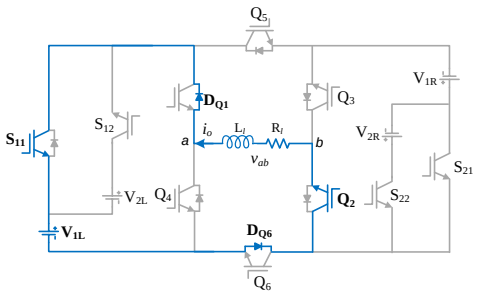
b) $V_{ab}=3V_{dc}$, $I_{out}(+)$



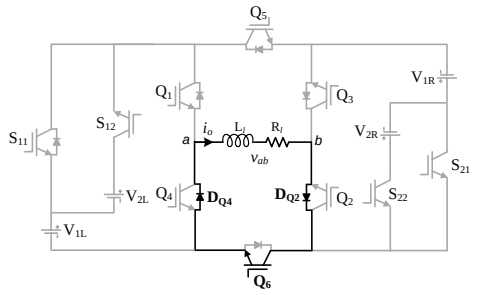
c) $V_{ab}=2V_{dc}$, $I_{out}(+)$



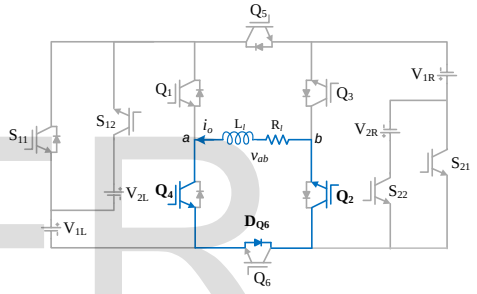
d) $V_{ab}=V_{dc}$, $I_{out}(+)$



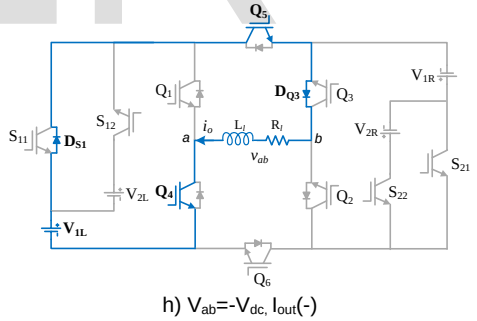
e) $V_{ab}=V_{dc}$, $I_{out}(-)$



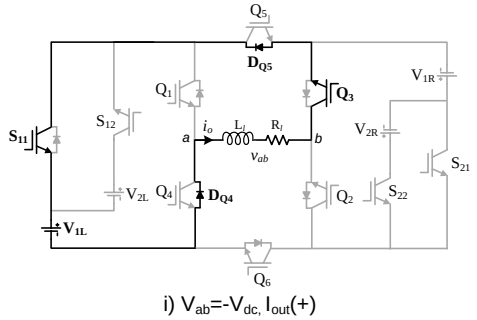
f) $V_{ab}=0$, $I_{out}(+)$



g) $V_{ab}=0$, $I_{out}(-)$



h) $V_{ab}=-V_{dc}$, $I_{out}(-)$



i) $V_{ab}=-V_{dc}$, $I_{out}(+)$

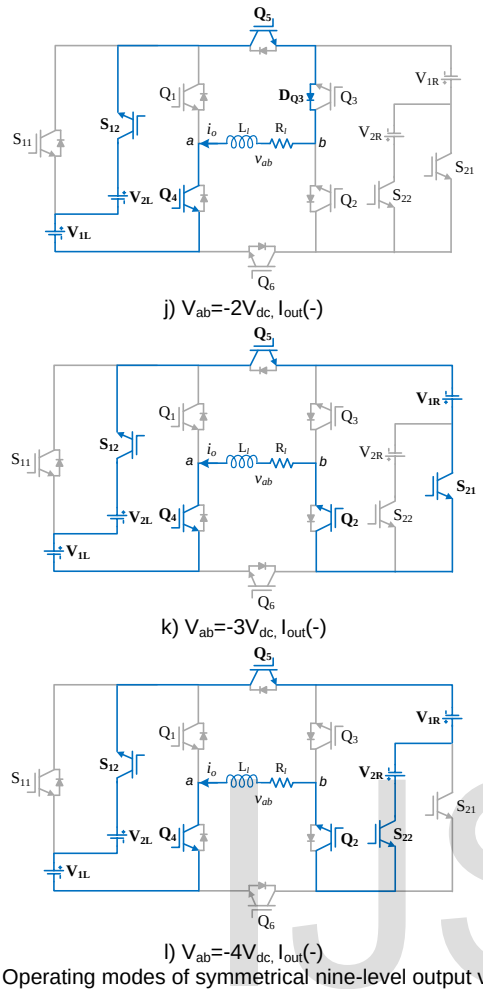


Fig. 2. Operating modes of symmetrical nine-level output voltage

2.2.2 Asymmetrical Dual-Module Multilevel Inverter

Asymmetrical configuration stands for values of DC voltage sources in Module-II will be unequal. Therefore, higher number of levels can be obtained which reduces the THD of the generated output voltage, while the same number of power components of symmetry topology is used. Based on two cells, β equals to '2'and '3' for asymmetrical operation as presented from (3) and the generated levels will be 13-level and 17-level, respectively as observed from (4). The switching states for asymmetrical operation based on two cells are presented in Table 2.

3 Modulation Scheme

Level shifted pulse width modulation technique (LSPWM) has been employed to generate the switching pattern. As shown in Fig. 3, the modulation scheme for MLI inverter is generated by comparing a rectified sinusoidal reference signal (V_{ref}) has a frequency of the required output voltage with triangle carrier signals. Carriers signal have the same switching frequency (F_{SW}), the same peak value but vary in offset voltage [21, 22]. Number of carrier signals (N_{car}) is determined by the following equation:

$$N_{car}=(N_{Levels}-1)/2 \quad (11)$$

TABLE 2
SWITCHING STATES OF ASYMMETRICAL DUAL-MODULE INVERTER

Voltage levels	13-level		17-level	
	Voltage magnitude	Switching states	Voltage magnitude	Switching states
$8V_{dc}$	-	-	$V_{1L}+V_{2L}+V_{1R}+V_{2R}$	S_{12}, Q_1, Q_3, S_{22}, Q_6
$7V_{dc}$	-	-	$V_{1L}+V_{1R}+V_{2R}$	D_{S11}, Q_1, Q_3, S_{22}, Q_6
$6V_{dc}$	$V_{1L}+V_{2L}+V_{1R}+V_{2R}$	S_{12}, Q_1, Q_3, S_{22}, Q_6	$V_{1R}+V_{2R}$	S_{22}, D_{Q4}, Q_3, Q_6
$5V_{dc}$	$V_{1L}+V_{1R}+V_{2R}$	D_{S11}, Q_1, Q_3, S_{22}, Q_6	$V_{1L}+V_{2L}+V_{1R}$	S_{12}, Q_1, Q_3, S_{21}, Q_6
$4V_{dc}$	$V_{1L}+V_{2L}+V_{1R}$	S_{12}, Q_1, Q_3, S_{21}, Q_6	$V_{1L}+V_{1R}$	D_{S11}, Q_1, Q_3, S_{21}, Q_6
$3V_{dc}$	$V_{1L}+V_{1R}$	D_{S11}, Q_1, Q_3, S_{21}, Q_6	V_{1R}	S_{21}, D_{Q4},Q_3, Q_6
$2V_{dc}$	$V_{1L}+V_{2L}$	S_{12}, Q_1, D_{Q2}, Q_6	$V_{1L}+V_{2L}$	S_{12}, Q_1, D_{Q2}, Q_6
$V_{dc}(+)$	V_{1L}	D_{S11}, Q_1,D_{Q2}, Q_6	V_{1L}	D_{S11}, Q_1,D_{Q2}, Q_6
$V_{dc}(-)$	V_{1L}	S_{11}, D_{Q1}, Q_2, D_{Q6}	V_{1L}	S_{11}, D_{Q1}, Q_2, D_{Q6}
0(+)	-	D_{Q2}, D_{Q4}, Q_6	-	D_{Q2}, D_{Q4}, Q_6
0(-)	-	Q_2, Q_4, D_{Q6}	-	Q_2, Q_4, D_{Q6}
$-V_{dc}(-)$	V_{1L}	D_{S11}, Q_4,D_{Q3}, Q_5	V_{1L}	D_{S11}, Q_4,D_{Q3}, Q_5
$-V_{dc}(+)$	V_{1L}	S_{11}, D_{Q4}, Q_3, D_{Q5}	V_{1L}	S_{11}, D_{Q4}, Q_3, D_{Q5}
$-2V_{dc}$	$V_{1L}+V_{2L}$	S_{12}, Q_4, D_{Q3}, Q_5	$V_{1L}+V_{2L}$	S_{12}, Q_4, D_{Q3}, Q_5
$-3V_{dc}$	$V_{1L}+V_{1R}$	D_{S11}, Q_4,Q_2, S_{21}, Q_5	V_{1R}	S_{21}, D_{Q1}, Q_2, Q_5
$-4V_{dc}$	$V_{1L}+V_{2L}+V_{1R}$	S_{12}, Q_4, Q_2, S_{21}, Q_5	$V_{1L}+V_{1R}$	D_{S11}, Q_4,Q_2, S_{21}, Q_5
$-5V_{dc}$	$V_{1L}+V_{1R}+V_{2R}$	D_{S11}, Q_4,Q_2, S_{22}, Q_5	$V_{1L}+V_{2L}+V_{1R}$	S_{12}, Q_4, Q_2, S_{21}, Q_5
$-6V_{dc}$	$V_{1L}+V_{2L}+V_{1R}+V_{2R}$	S_{12}, Q_4, Q_2, S_{22}, Q_5	$V_{1R}+V_{2R}$	S_{22}, D_{Q1}, Q_2, Q_5
$-7V_{dc}$	-	-	$V_{1L}+V_{1R}+V_{2R}$	D_{S11}, Q_4,Q_2, S_{22}, Q_5
$-8V_{dc}$	-	-	$V_{1L}+V_{2L}+V_{1R}+V_{2R}$	S_{12}, Q_4, Q_2, S_{22}, Q_5

The intersection points between carrier signals with V_{ref} decide the output voltage levels. The positive half-cycle of V_{ref} is responsible for generating positive levels while the rectified half-cycle of V_{ref} is responsible for generating negative levels. Modulation has been designed with carrier frequency of 10 kHz, whereas the reference signal frequency is kept at 50 Hz.

4 Simulation Results

System simulation is used to validate the performance of the proposed topology using the MTLAB/SIMULINK. Simulation parameters are listed in Table 3. Switching frequency of LSPWM is taken as 10 kHz. An important measuring of MLI performance is the harmonic spectrum for the inverter output voltage as it provides the harmonic amount in the generated

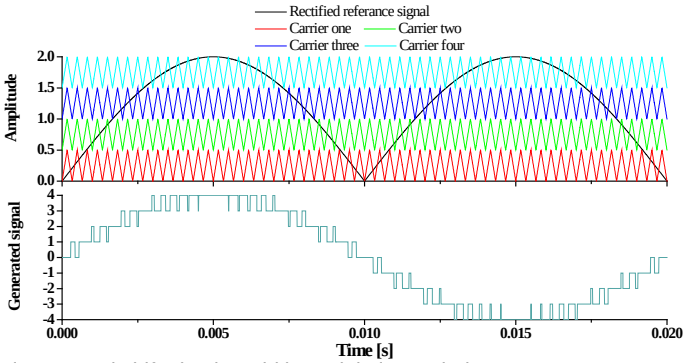


Fig. 3. Level shifted pulse width modulation technique

voltage. Fig. 4 presents simulation results for 9-level dual-module scheme based on symmetry topology with two cells. The inverter output voltage is shown in Fig. 4(a), while Fig. 4(b) presents the harmonic spectrum of inverter output voltage. In Fig. 5 the output voltage with 13-level results are presented. Fig. 5(a) provides the 13-level inverter output voltage and harmonic spectrum is given in Fig. 5(b) for inverter output voltage. As seen from Fig. 4(b) and Fig. 5(b), low harmonic content is introduced in 13-level as the number of levels increases which significantly leads to less filters.

Also, a major concern for MLI operation is the total harmonic distortion (THD) which can be used to measure how close the output voltage to its sinusoidal reference. It can be calculated as follows:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \quad (12)$$

Where, V_1 represents RMS value of fundamental component of output voltage while, V_n represents RMS value of nth harmonic component. THD must meet the host requirements of value less than 5% according to the IEEE-519 standard. The THD of inverter output voltage for 9-level is equal to 13.93 % up to 100 kHz while is found to be 9.3% in case of 13-level. This value can be reduced to meet the requirements by using small passive filler in size.

TABLE 3
SIMULATIN PARAMETERS

Parameter		Variable	Value
Input DC voltage source (Peak)	9-level	V_{1L}= V_{2L}	15 V
		V_{1R}= V_{2R}	15 V
	13-level	V_{1L}= V_{2L}	15 V
		V_{1R}= V_{2R}	30 V
Power frequency		F	50 Hz
Switching frequency		F_{SW}	10 kHz
Load		R	72 Ω

5 REAL TIME VALIDATION

The performance of the proposed dual-module inverter with a real-time (RT) setup has been performed and compared with simulation results. RT simulation is implemented using MATLAB/SIMULINK and dSAPCE-CP1103 control desk. The RT results are illustrated in Fig. 6 with the same parameters used in the simulation. The inverter output voltage is displayed in Fig. 9 (a) and Fig. 9 (b) for 9-level and 13-level, respectively.

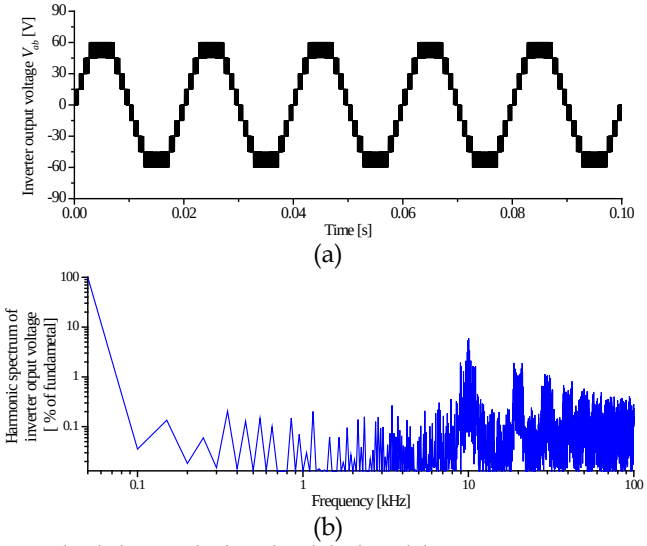


Fig. 4. Simulation results for 9-level dual-module MLI

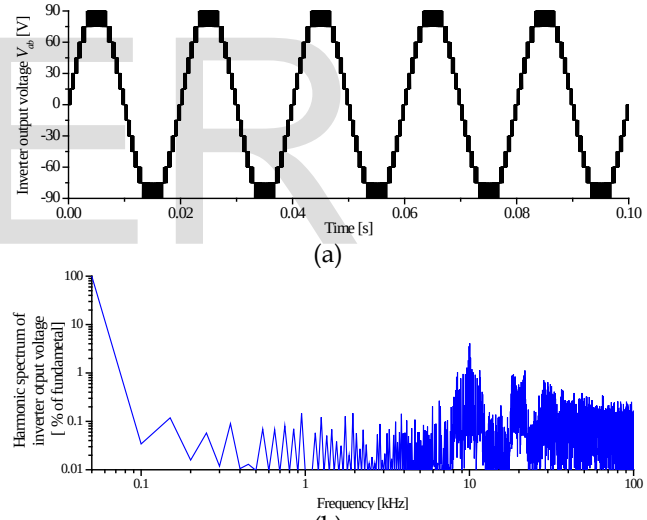
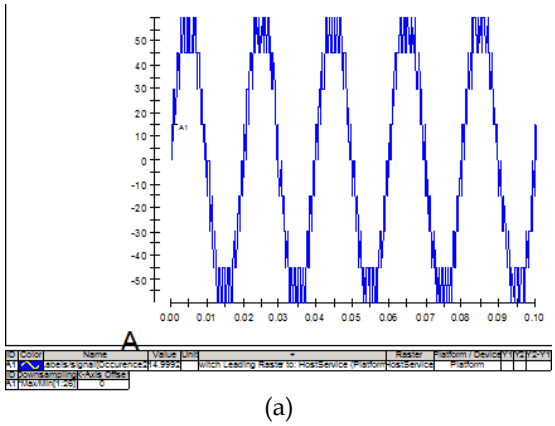
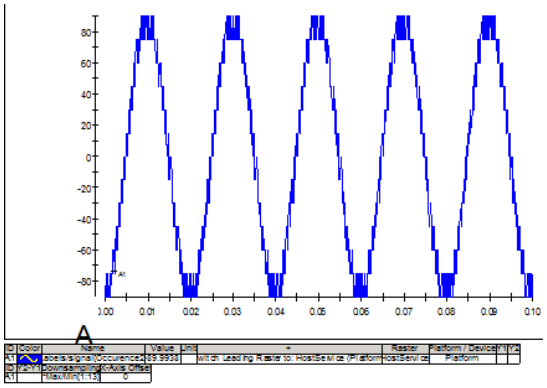


Fig. 5. Simulation results for 13-level dual-module MLI


(a)



(b)

Fig. 6. Real-time results of the proposed dual-module MLI

6 Comparisons with Other Topologies

To present the effectiveness of the proposed topology, a comparison must be made between the proposed topology with recent topologies. Table 4 presents a comparison between different nine-level topologies with the proposed topology. The comparison is made under the following parameters; N_{DC}, N_{Sw}, number of clamping capacitors (N_c), number of diodes (N_D), and total number of components (N_T). In addition, the parameter number of level to power switch ratio (LS ratio) is calculated. As this value increased, the cost, losses and efficiency of the presented topology will improved. It is obvious that TSV in the proposed nine-level inverter in dual is higher than MLIs presented in [14], [24]. Therefore, it is the disadvantage of the proposed inverter but it is still have advantages in comparison with the presented topologies. As in [14], the presented topology has higher number of components which increases the total cost and losses compared with the proposed topology. in case of symmetry 13-level in [24], the presented topology offers fourteen switches while in the proposed topology based on symmetry operation from (4), offers only twelve power switches. In that case it will show an inefficient operation at higher levels.

TABLE 4
COMPARATIVE ANALYSIS TO OBTAIN SYMMETRICAL SINGLE-PHASE NINE-LEVEL INVERTER

Ref.	Components						
	N_{DC}	N_{SW}	N_C	N_D	N_T	*LS* RATIO	*TSV*/V_{DC}
[15]	1	16	8	30	55	0.5625	28
[14]	4	16	0	0	20	0.5625	16
[23]◉	4	10	0	3	17	0.90	33
[24]◉	4	10	0	0	14	0.9	16
PROPOSED	4	10	0	0	14	0.90	20

7 Conclusion

A new single-phase multilevel inverter was recommended in this paper with a low number of components. The proposed dual-module topology was presented which can be operated in symmetrical or asymmetrical configurations. The proposed topology was presented to generate 9/13level and THD was calculated and showed low value of 7 % at 13-level. A comparison has been made with the proposed topologies and recent topologies mainly on total number of components, level to switch ratio, and total standing voltage. The proposed dual-module presented its effectiveness in case of lower number of components and low value of level to switch ratio at higher number of levels. Simulation and real time results were taken to show the effectiveness of the proposed inverter.

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